

Supercomputers in Nagoya University



KATSUYA ISHII

The Information Technology Center (ITC) of Nagoya University was originally established as the Computing Center of Nagoya University, which all researchers of academic organization in Japan can used.

The first supercomputer of Nagoya University was Fujitsu supercomputer VP100(250Mflops) installed in the Institute of Plasma Physics in January 1984, which was the first operated supercomputer in Japan.

High Performance Computing Infrasturacture of Japan

<http://www.hpci-office.jp/folders/english>

HPCI

What is HPCI?

HPCI is a innovative common computational infrastructure responding to diversified needs of the users. It consists of K computer and other supercomputers installed in universities and research institutions in Japan connected by high speed back-bone networks.



Example

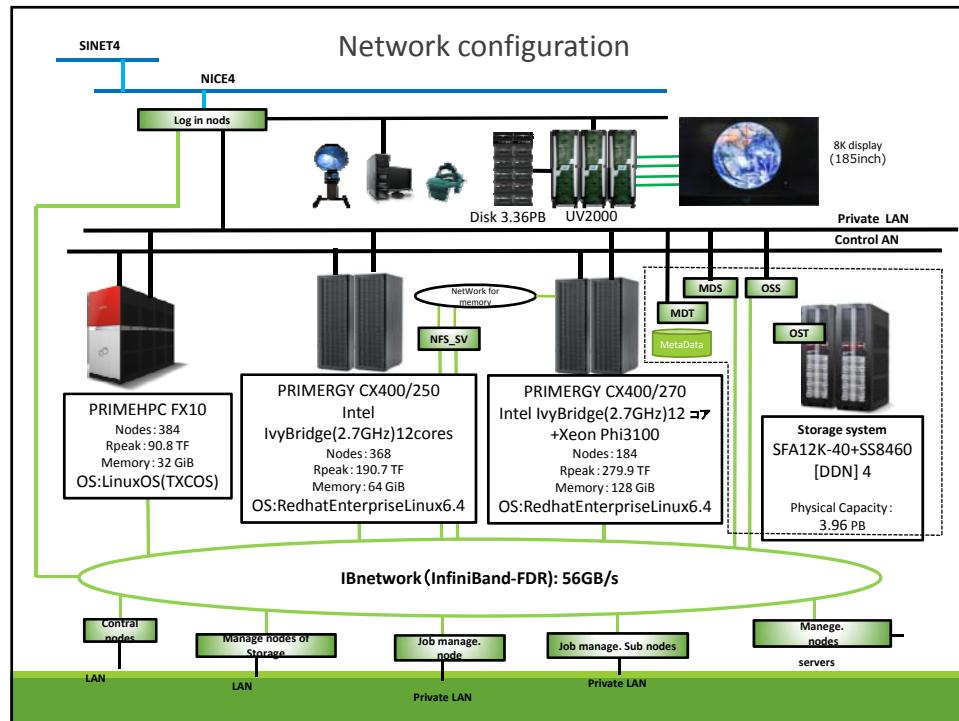
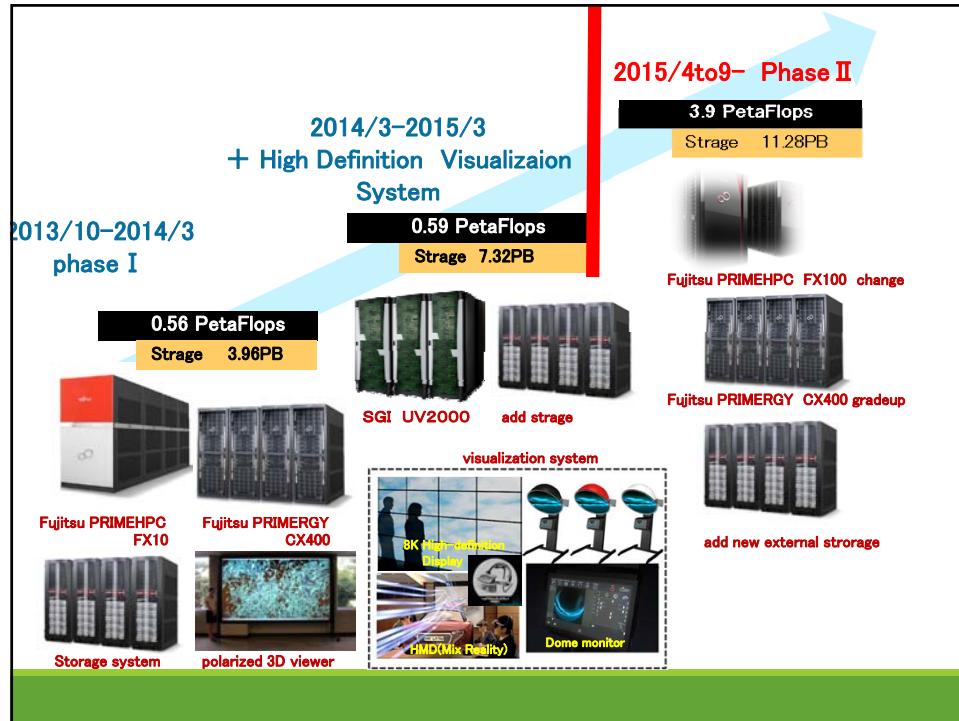
1. The K computer (named for the Japanese word “kei” (京), meaning 10^{16}) Fujitsu 88,128 SPARC64VIIIfx's at the RIKEN Advanced Institute for Computational Science , Kobe.

11.28Petaflops (4th of Top500)

* TIT : Tsubame 2.5: Xeon+GPU 5.375Petaflops

* U. Tokyo : Fujitsu FX10 SPARC64IXfx's
4,800nodes 1.135Petaflops

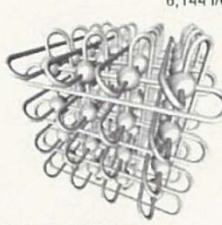
* Tohoku Univ. : NEC SX-ACE 2,560nodes
etc 0.707Petaflops



FX10

<http://img.jp.fujitsu.com/downloads/jp/jhpc/primehpc/primehpc-fx10-catalog-en.pdf>

PRIMEHPC FX10 Specifications

  <p>6,144 I/O</p> <p>Tofu Interconnect Topology (Conceptual Diagram)</p> <p>■ VISIMP Hybrid pa...</p>	Node specifications <table border="1" style="width: 100%; border-collapse: collapse;"> <tbody> <tr><td>Theoretical peak performance</td><td>236.5 Gigaflops</td></tr> <tr><td>Processor</td><td>SPARC64 IXfx (1.848 GHz/16-core) x1</td></tr> <tr><td>Memory capacity</td><td>32GB, 64GB</td></tr> <tr><td>Memory bandwidth</td><td>85 GB/s</td></tr> <tr><td>Interconnect link bandwidth</td><td>5 GB/s x2 (bi-directional)</td></tr> </tbody> </table> System specifications <table border="1" style="width: 100%; border-collapse: collapse;"> <tbody> <tr><td>Number of racks</td><td>4 to 1,024</td></tr> <tr><td>Number of compute nodes</td><td>384 to 98,304</td></tr> <tr><td>Theoretical peak performance</td><td>90.8 Tflops to 23.2 Pflops</td></tr> <tr><td>Total memory capacity</td><td>1.2TB to 6PB</td></tr> <tr><td>Interconnect</td><td>Tofu Interconnect</td></tr> <tr><td>Cooling method</td><td>Direct water cooling + air cooling (Option: Exhaust cooling unit)</td></tr> </tbody> </table>	Theoretical peak performance	236.5 Gigaflops	Processor	SPARC64 IXfx (1.848 GHz/16-core) x1	Memory capacity	32GB, 64GB	Memory bandwidth	85 GB/s	Interconnect link bandwidth	5 GB/s x2 (bi-directional)	Number of racks	4 to 1,024	Number of compute nodes	384 to 98,304	Theoretical peak performance	90.8 Tflops to 23.2 Pflops	Total memory capacity	1.2TB to 6PB	Interconnect	Tofu Interconnect	Cooling method	Direct water cooling + air cooling (Option: Exhaust cooling unit)
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Band width/Flops = 0.36Byte/Flops

CX400 systems

Fujitsu Primergy CX400	
OS	Red Hat Enterprise Linux 6.4
Processor	Intel IvyBridge (2.7GHz) 12 core
Number of Nodes	552(13,248 cores)
Total Peak Performance	470.6Tflops
Total memory capacity	43TiB
Peak Performance of a node	518Gflops(24core)
Memory capacity of a node	64GiB(270)/128GiB(250)

coprocessor	
Xeon Phi3100 family(MIC)	
Processor	Accelerator(Pcie G2) 1.1GHz 57cores
Number of Nodes(cores)	184(10,488cores)
Peak performance of a node	1,003Gflops(57cores)
Memory capacity of a node	6GiB

Examples of Matrix multiplication
(Block method) $C=AB \quad 10^4 \times 10^4$

$$\begin{pmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{pmatrix} \begin{pmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{pmatrix} = \begin{pmatrix} A_{11}B_{11} + A_{12}B_{21} & A_{11}B_{21} + A_{12}B_{22} \\ A_{21}B_{11} + A_{22}B_{21} & A_{21}B_{21} + A_{22}B_{22} \end{pmatrix} = C$$

Table 3.3: Result for Matrix Multiplication: Host vs Coprocessor

System	Time(sec)	Performance(GFLOPS)
Host(1 core,Non-parallelized)	404.003	4.950
Host(OMP 4 cores, 4 threads)	98.990	20.204
Host(OMP 8 cores, 8 threads)	49.827	40.139
Host(OMP 12 cores, 12 threads)	33.228	60.190
Host(OMP 16 cores, 16 threads)	24.841	80.513
Host(OMP 24 cores, 24 threads)	16.703	119.737
Xeon Phi(OMP 224 threads scatter)	10.947	170.151
Xeon Phi(OMP 224 threads compact)	9.981	186.619

Batch Job

	JOB CLASS	Nodes	Cores	Max usable time		Memory	
				Default (Hours)	Max (Hours)		
Fx10	fx-interactive	1	16	1	1	28GiB	For Deug
	fx-debug	4	64	1	1	28GiB × 4	
	fx-small	12	192	24	72	28GiB × 12	
	fx-middle	48	768	24	72	28GiB × 48	
	fx-large	96	1,536	24	72	28GiB × 96	
	fx-special	384	6,144	unlimited		28GiB × 384	consult
Cx400/250	cx-debug	4	96	1	1	56GiB × 4	For Debug
	cx-single	1	24	24	336	56GiB × 1	
	cx-small	8	192	24	168	56GiB × 8	
	cx-middle	32	768	24	168	56GiB × 32	
	cx-large	128	3,072	24	72	56GiB × 128	
	cx-special	368	8,832	unlimited		56GiB × 368	consult
Cx200/270	cx2-debug	4	96	1	1	112GiB × 4	For Debug
	cx2-small	8	192	24	72	112 GiB × 8	
	cx2-middle	32	768	24	72	112 GiB × 32	
	cx2-large	64	1,536	12	12	112 GiB × 64	
	cx2-special	184	4,416	Unlimited		112GiB × 184	consult

2nd Floor

- SuperComputer FX10
- Front end Machine (Login node)
- Storage System



3rd Floor

- Supercomputer CX400



	First Phase 2013.10～	Second Phase 2015.4～2018.3
SystemI Fujitsu Sparc	FX10: 0.1 PFLOPS	FX100: 3.2PetaFLOPS
System II Intel CPU	CX400: 0.47 PFLOPS	CX400: 0.68 PFLOPS
Storage	3.96 PB	7.92 PB

FX100 architecture (New Fujitsu SC)

An expansion to the SPARC-V9 instruction set architecture called HPC-ACE2 (High Performance Computing-Arithmetic Computational Extensions 2) features two 256-bit wide SIMD units per core with advanced operation functions, and improves the computational throughput of the processor. HMC (Hybrid Memory Cube) allows a high memory bandwidth of 480GB/s per node and the one-processor-per-node architecture exploits the maximum memory performance. Tofu Interconnect 2 (Tofu2) is integrated into the SPARC64 XIfx processor and enhances node-to-node communication bandwidth to 12.5 GB/s per link with lower latency. Highly scalable Tofu2 enables a system configuration of over 100,000 nodes.

BF=0.48Byte/flops

<http://img.jp.fujitsu.com/downloads/jp/jhpc/primehpc/primehpc-fx100-datasheet-en.pdf>

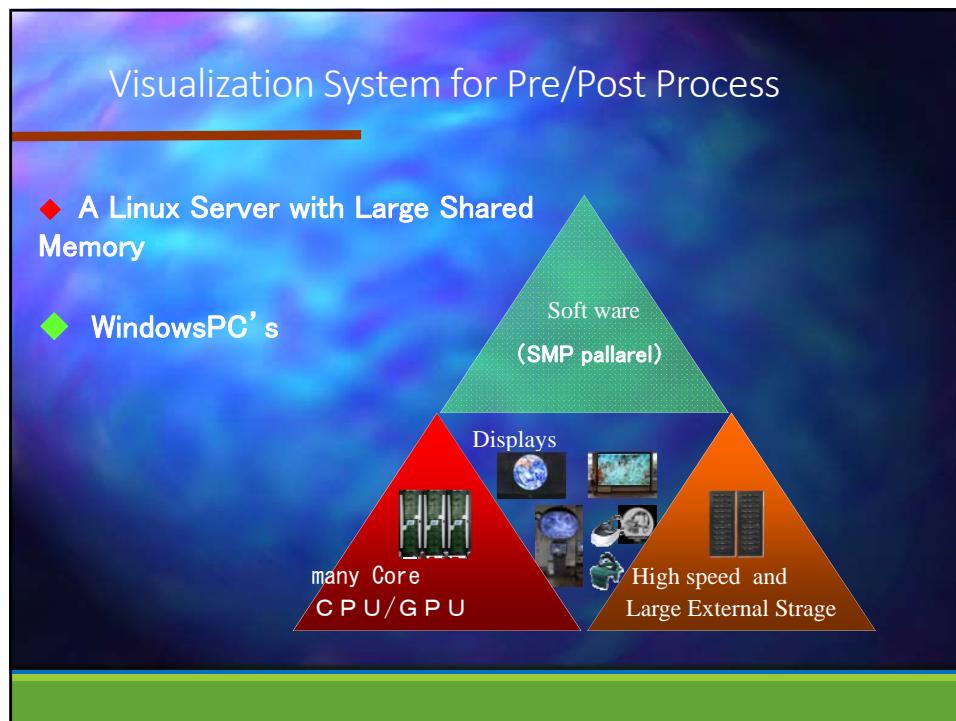
FUJITSU Supercomputer PRIMEHPC FX100 Specifications		
2,880nodes		
	CPU	Processor SPARC64 XIfx
	CPU	Architecture SPARC V9 + HPC-ACE2
	CPU	No. of cores 32 compute cores + 2 assistant cores
	CPU	Theoretical peak performance Over 1 teraflops (double precision)
	Node	Architecture 1 CPU per node
		Memory capacity 32 GB (HMC)
		Memory bandwidth 240 GB/s (read) + 240 GB/s (write)
		Interconnect Tofu Interconnect 2
	Main unit	Interconnect link bandwidth 12.5 GB/s x 2 (bi-directional) per link
		Form factor 19-inch 2U
		No. of nodes 12
	System rack	No. of main units Up to 18 (216 nodes per rack)
	Maximum configuration	No. of nodes Over 100,000
		Theoretical peak performance Over 100 petaflops (double precision)
		Total memory capacity Over 3 PB

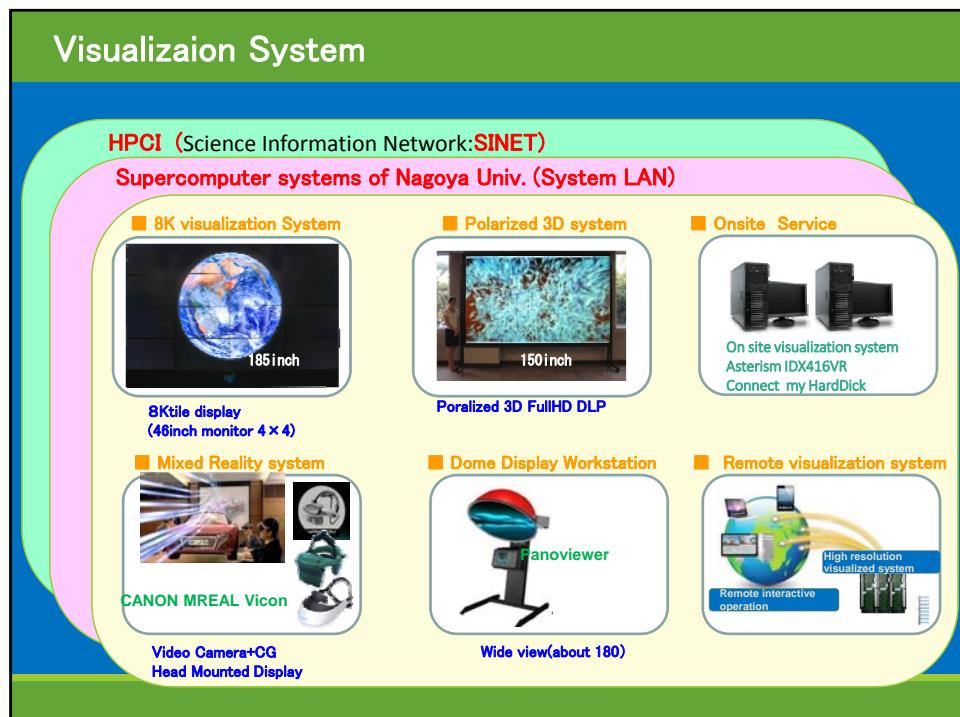
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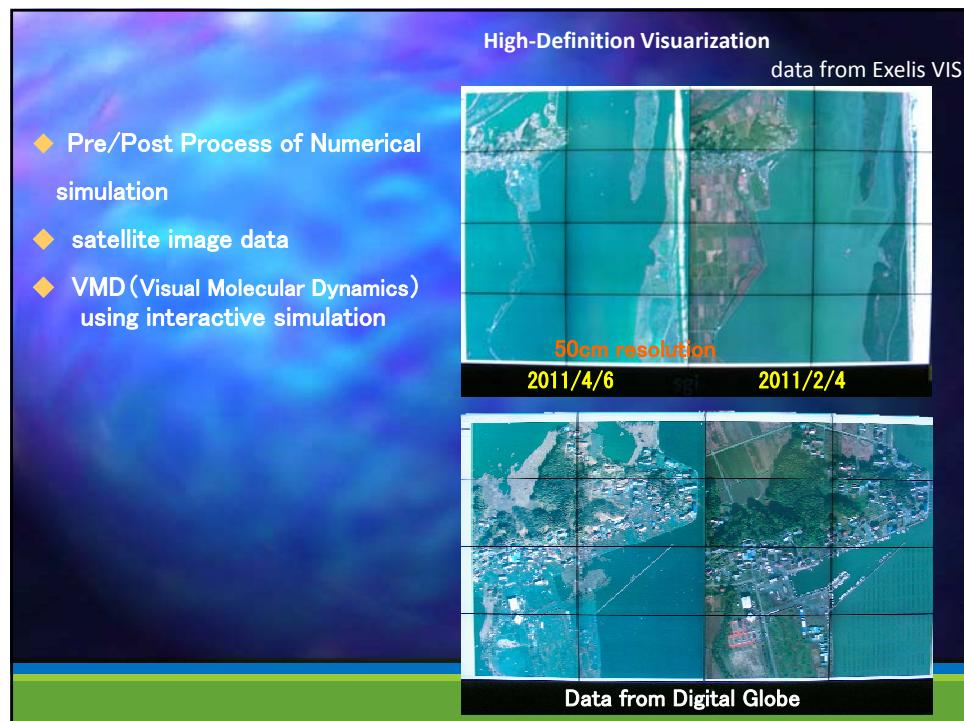
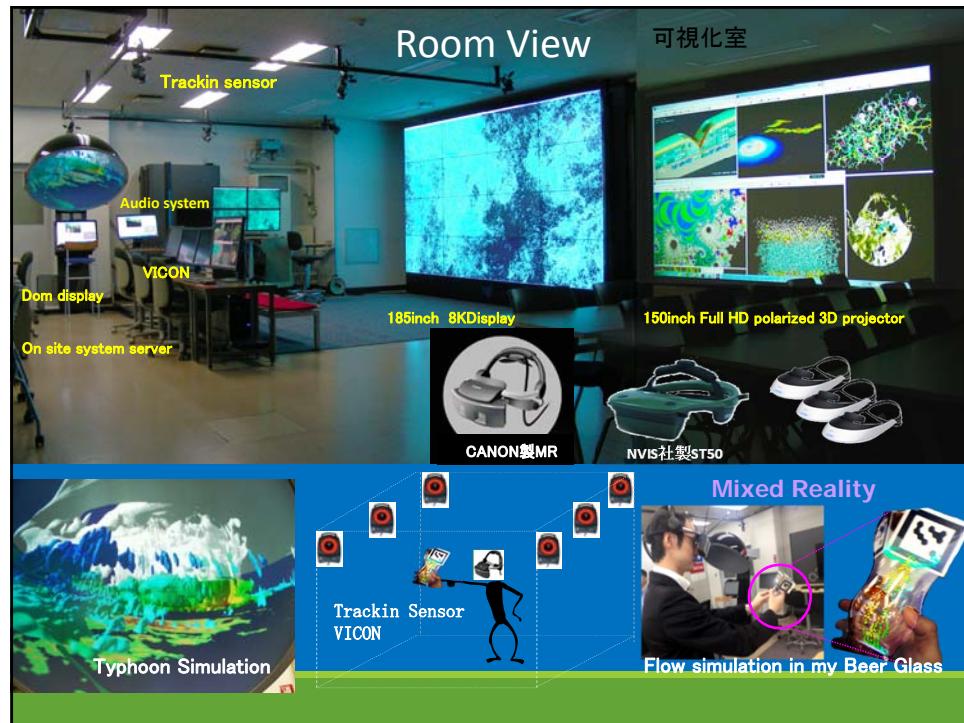
CX400/2550 systems	
	Fujitsu Primergy CX400
OS	Red Hat Enterprise Linux
Processor	Intel Haswell
Number of Nodes	400
Total Peak Performance	400Tflops
Total memory capacity	51.2TiB
Peak Performance of a node	1Tflops
Memory capacity of a node	128GiB

CX400/270 systems	
	Fujitsu Primergy CX400
OS	Red Hat Enterprise Linux 6.4
Processor	Intel IvyBridge (2.7GHz) 12 core
Number of Nodes	184(4,416cores)
Total Peak Performance	96Tflops
Total memory capacity	
Peak Performance of a node	518Gflops(24core)
Memory capacity of a node	128GiB

coprocessor	Xeon Phi3100 family(MIC)
Processor	Accelerator(Pcle G2) 1.1GHz 57cores
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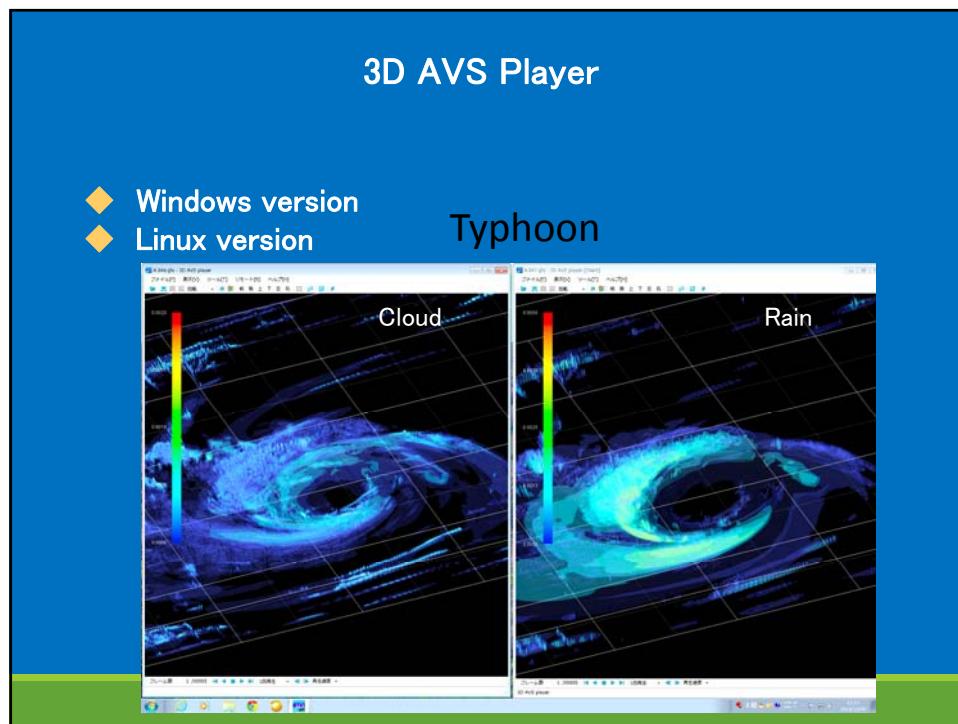
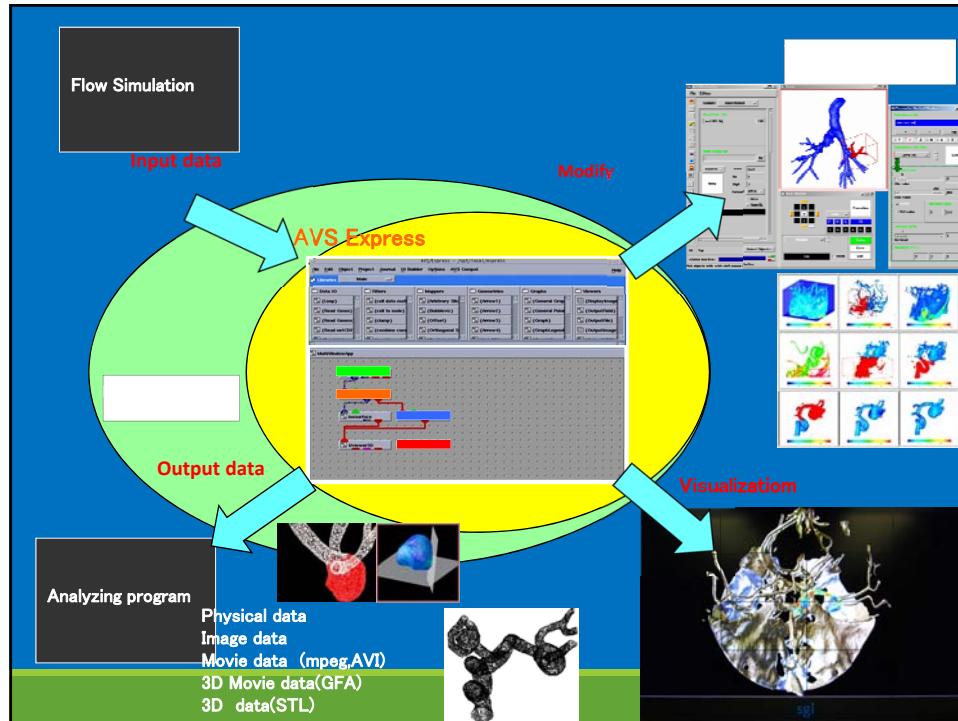


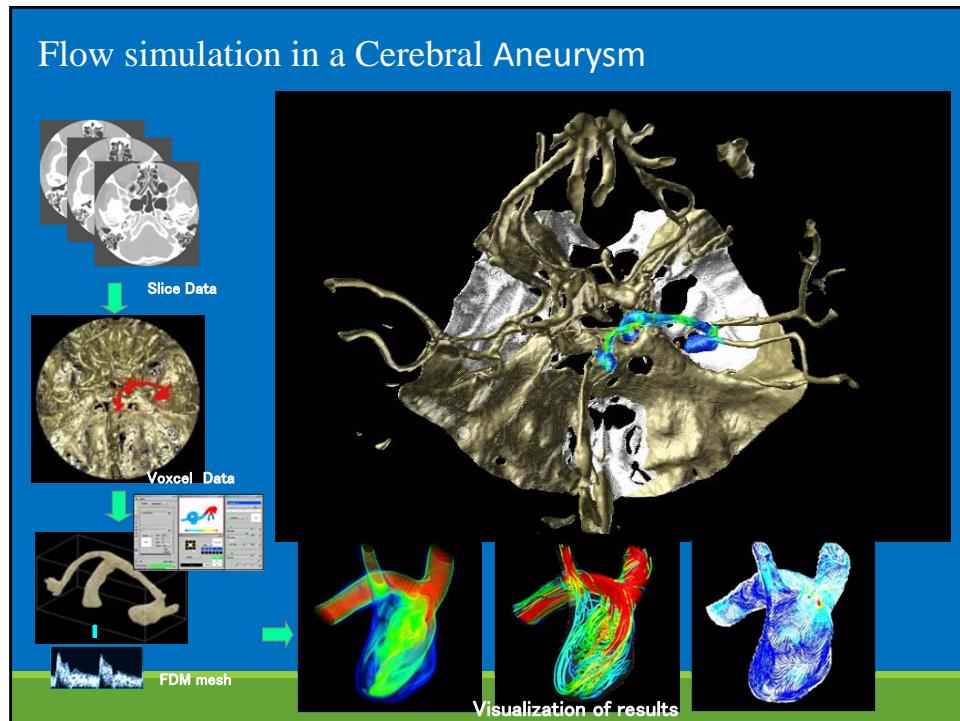




SGI UV2000 Software	
システム名	SGI UV 2000
OS	SuSE Linux Enterprise Server 11
Development	Intel Composer XE 14.0.1
Math Library	Intel MKL 11.1
MPI	SGI MPT 2.08
Batch	PBS Professional 12.2
Softwares for Visualization	AVS Express Developer PCE Ensight DR ParaView (parallel) IDL、ENVI
Software for remote 3D visualization	SGI NICE DCV 2013.0
Others	POV-Ray (SMP対応版) ffmpeg, ffplay, osgviewer, VMDなど
Fourier Transformation	FFTW 3.3
I/O library	HDF5 1.8.2, netcdf 4.2.1

Visualization Examples





Acknowledgment

- ◆ FUJITSU
- ◆ SGI Japan
- ◆ NVIDIA
- ◆ CYBERNET SYSTEMS
- ◆ Exelis VIS